Heavy Photon Search DAQ and Trigger

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Requirements

- 50kHz event rate at Event Builder
- 250MB/s data rate at Event Builder (calorimeter 25MB/s, muon 6MB/s, SVT 215MB/s)
- 100MB/s data rate on tape (after level3 trigger)

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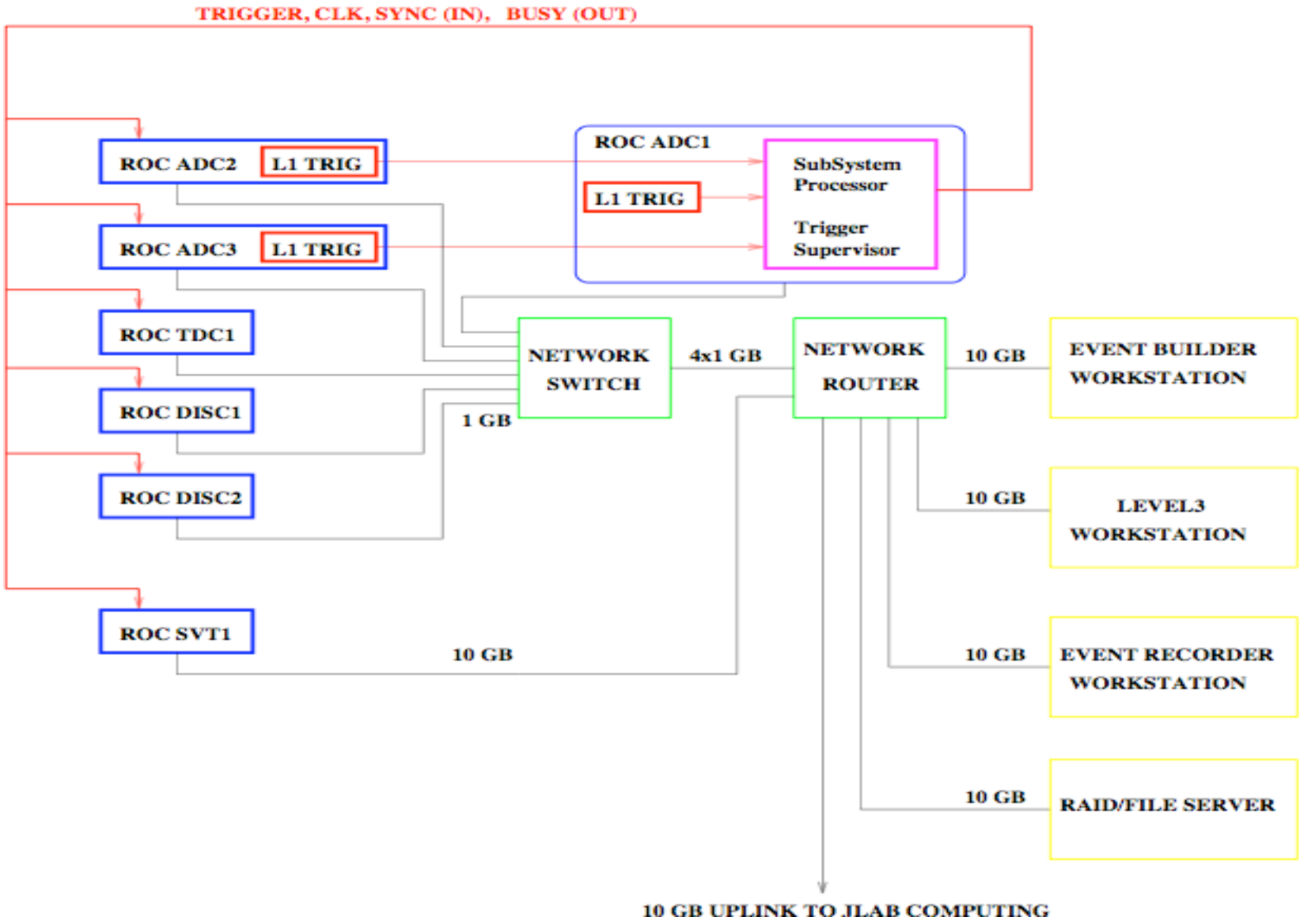
DAQ System Overview



DAQ System Overview (cont.)

- SVT readout system: 10 boards in ATCA format
- Calorimeter and Muon System Readout: 704 channels of 12bit 250MHz Flash ADCs, 144 channels of 85ps resolution pipeline TDCs with discriminators
- Flash ADC - based trigger system
- 2 VME, 1 VME64X, 3 VXS, 1 ATCA crates equipped with Readout Controllers and Trigger Units
- JLAB CODA DAQ software

SVT Data Rate

- The assumption is that the system will run at 3 times the noise threshold.
- The occupancy is thus 0.135%.
- This occupancy results in 92 SVT channels over threshold.
- From legitimate tracker hits 10 x 2(strips/layer) x2 (H&V) x 6 layers= 240 channels are expected.
- Each channel-over-threshold results in 6 digitized values (one mode available in the APV25)
- Including headers, etc, the resulting data rate is 4,316 bytes x 50 KHz = 215.8 Mbytes/sec from SVT after data reduction in ATCA FPGA's.

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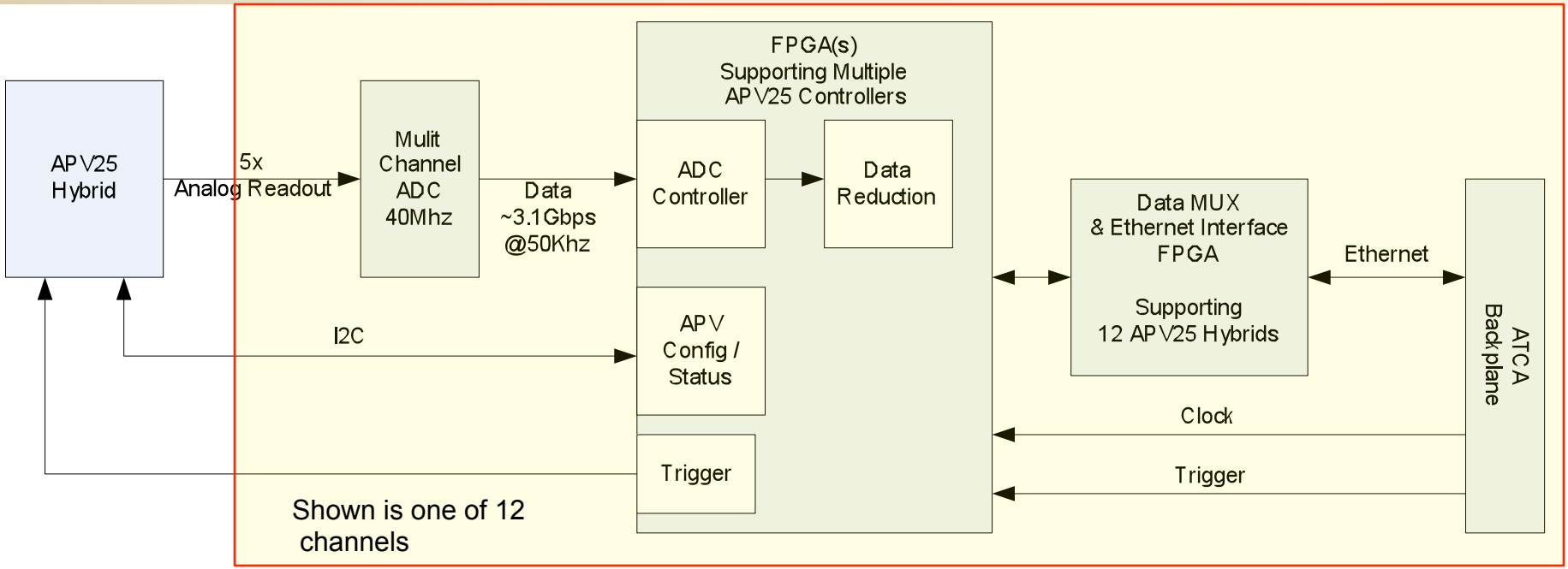
ATCA (Advanced Telecommunications Computing Architecture)
SVT Readout Board (SLAC)



- Each board supports 12 Hybrids Containing 5 APV25s each
- Total data input = ~36.9Gbps
- Data reduction performed on incoming data in FPGA
- Output data rate depends on occupancy
  - Expected rate <= 2Gbps (from last slide) total for 10 cards
  - Capability of ATCA systems running at SLAC is 10 Gbit/s per card, up to 100 Gbit/sec communication within a crate, 20 Gbit/sec off the crate
- System clock & trigger received from ATCA backplane
- 10Gbps Ethernet backplane interconnect

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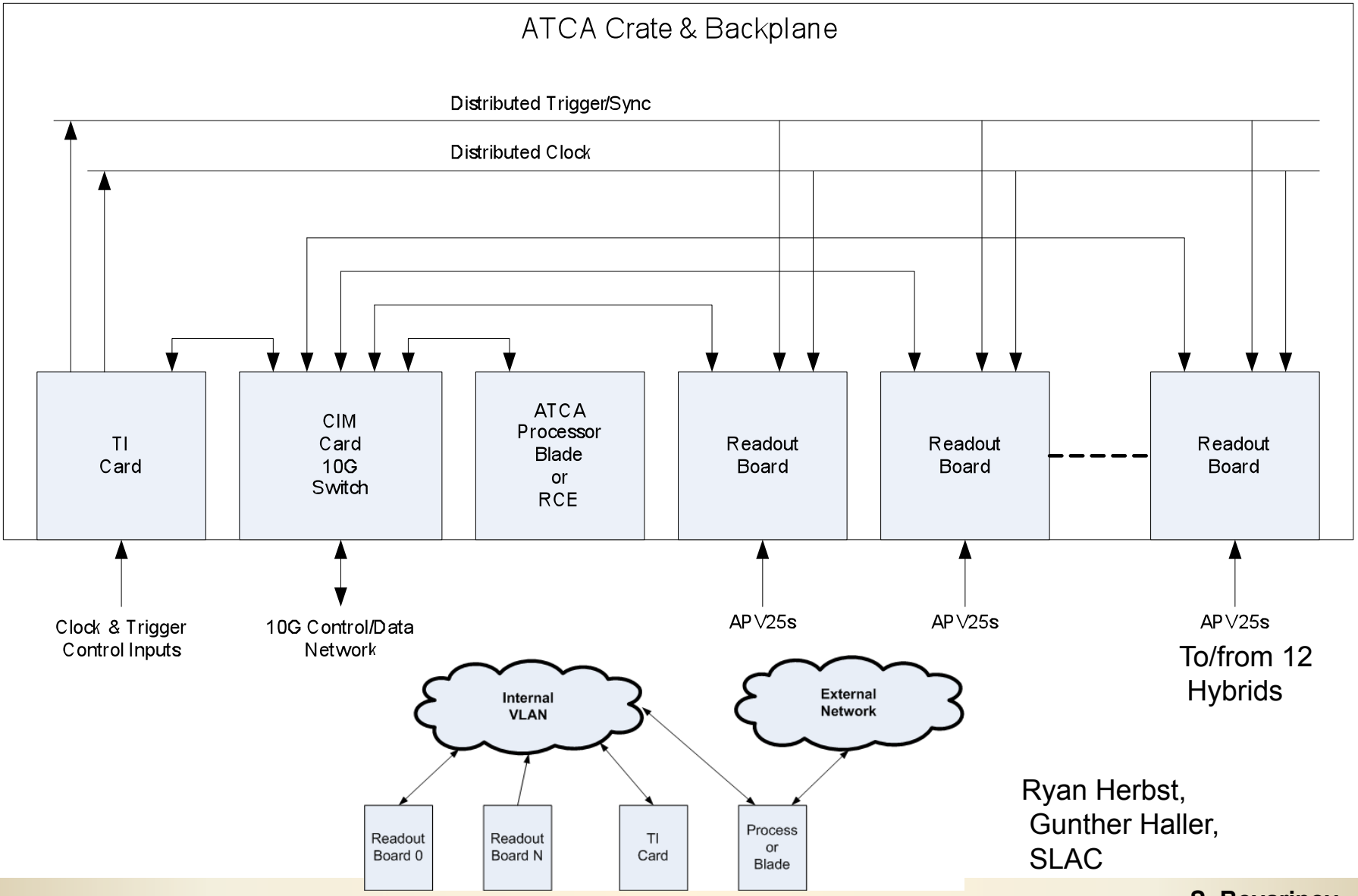
Gunther Haller,
SLAC

ATCA SVT Readout System (SLAC)



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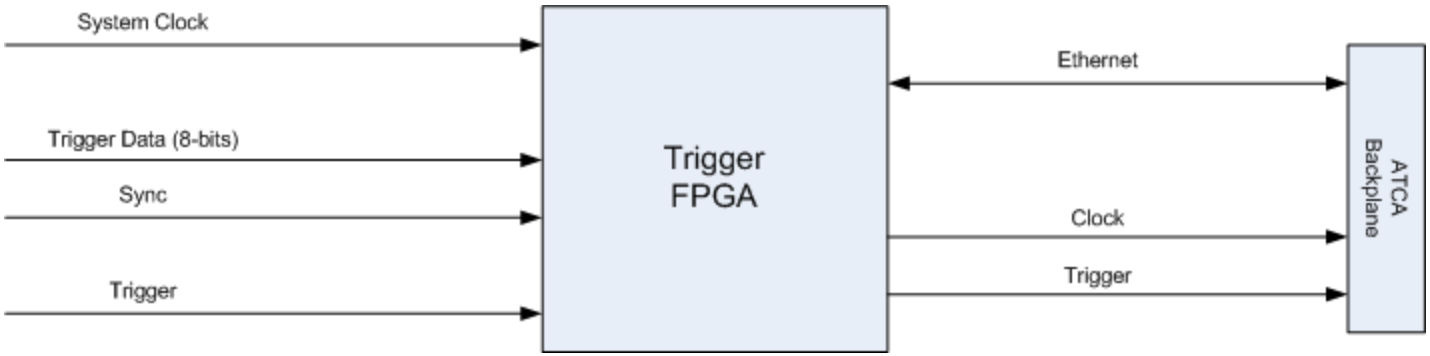
SVT Trigger Interface Board (SLAC)



- Receives clock, trigger & sync from trigger supervisor
  - Forwards signals to readout boards over ATCA backplane
- Forwards buffer control information to CPU over Ethernet
- Functionality may be combined into readout board design if space permits
  - One readout board would be assigned the role of trigger interface
- Duplicate of existing TI design in ATCA format
  - Addition of Ethernet interface for management

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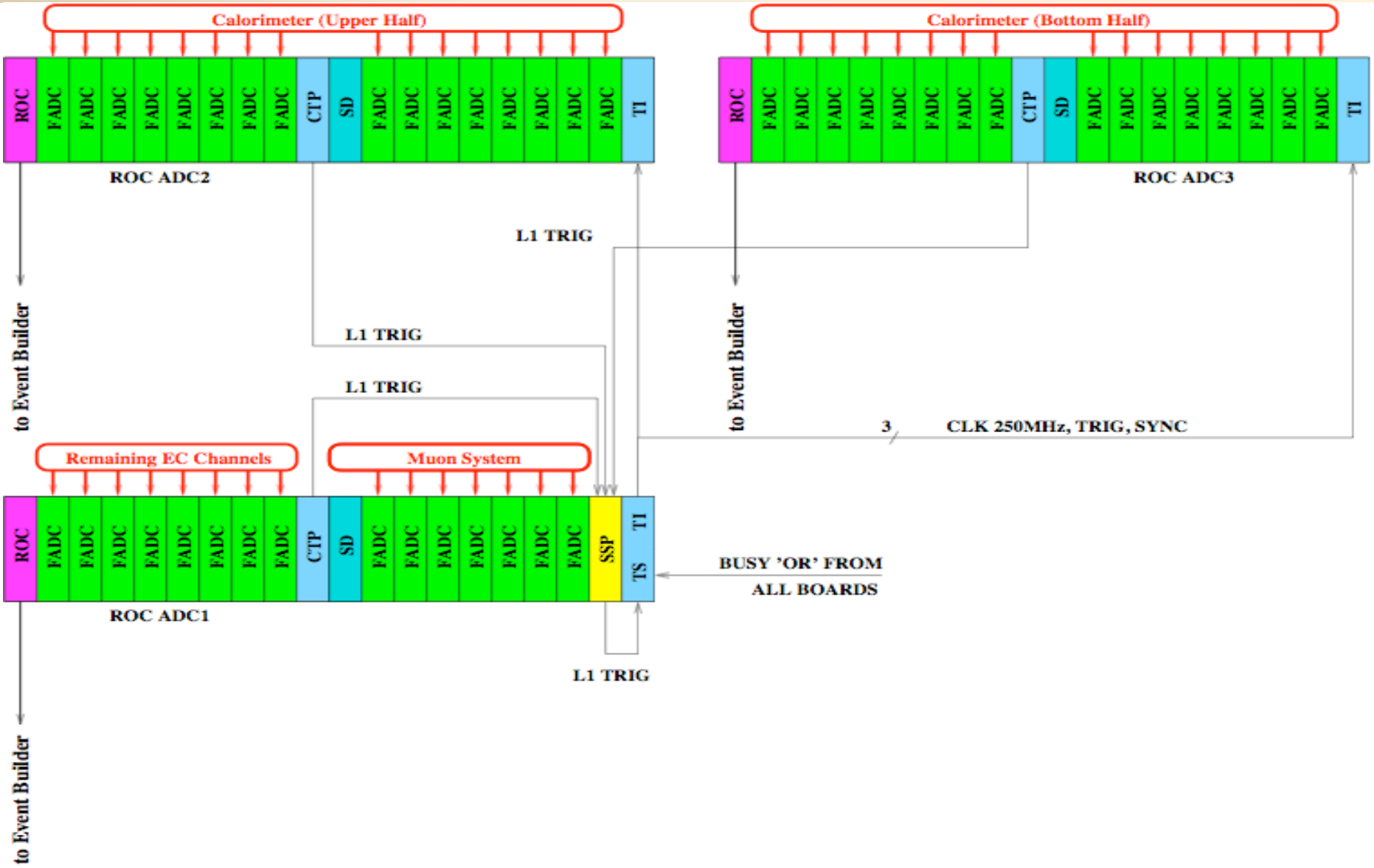
Flash ADC and Trigger System (VXS)



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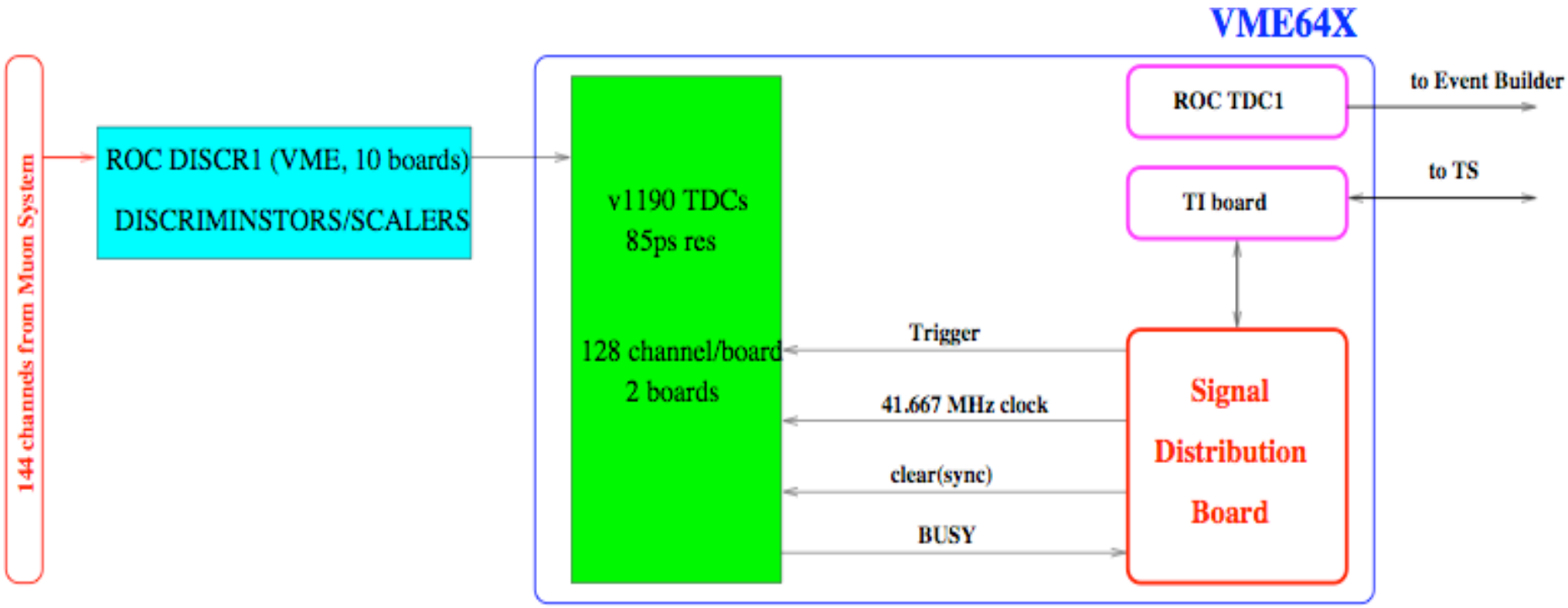
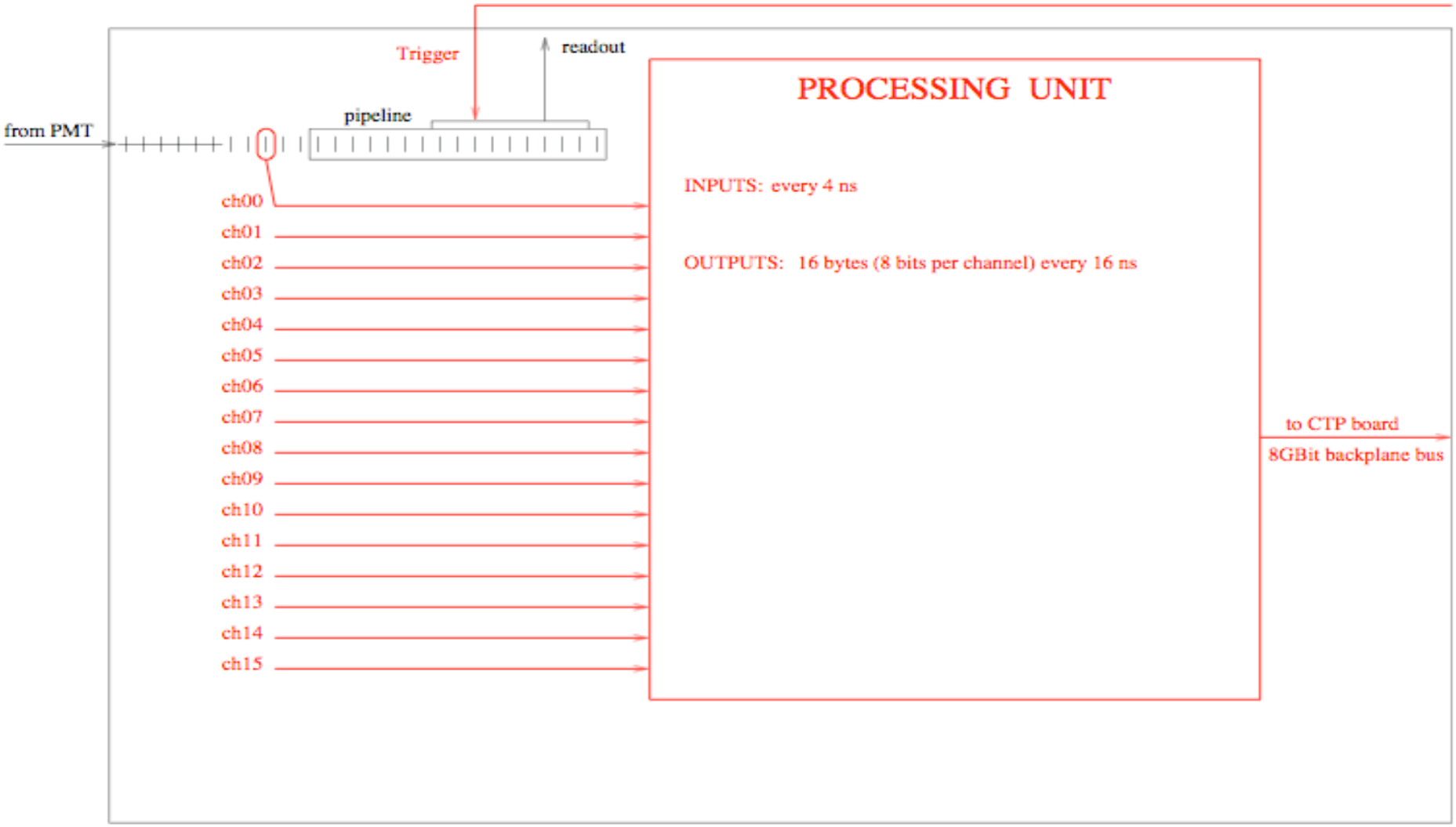
Pipeline TDC System (VME64X/VME)



Trigger processing - FADC

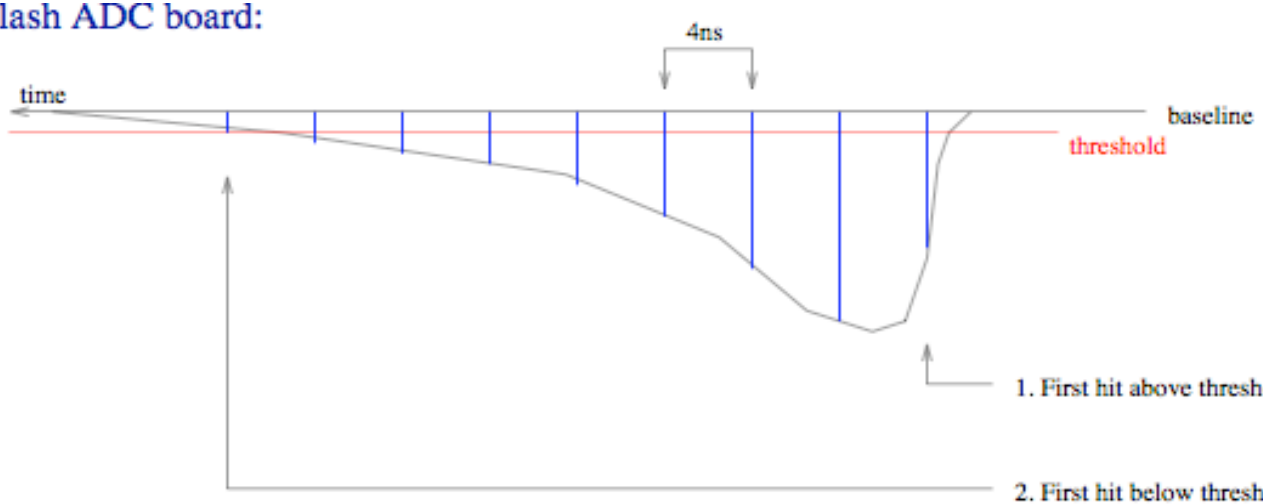


NOTES:
– only channel 00 is shown in details, all other channels have the same structure

Flash ADC board data processing logic

Trigger processing - FADC (cont.)

Flash ADC board:



1. First hit above threshold: start sum window, add previous hit to it

2. First hit below threshold: add that hit to the window, close window; we have now ADC value and WINDOW_SIZE

3. Wait DELAY ns and send ADC valie to the CTP board (DELAY = DELAY0 – WINDOW_SIZE, where DELAY0 is delay constant for all channels, order of 128ns; this way sending time will be related to the beginning of the window)

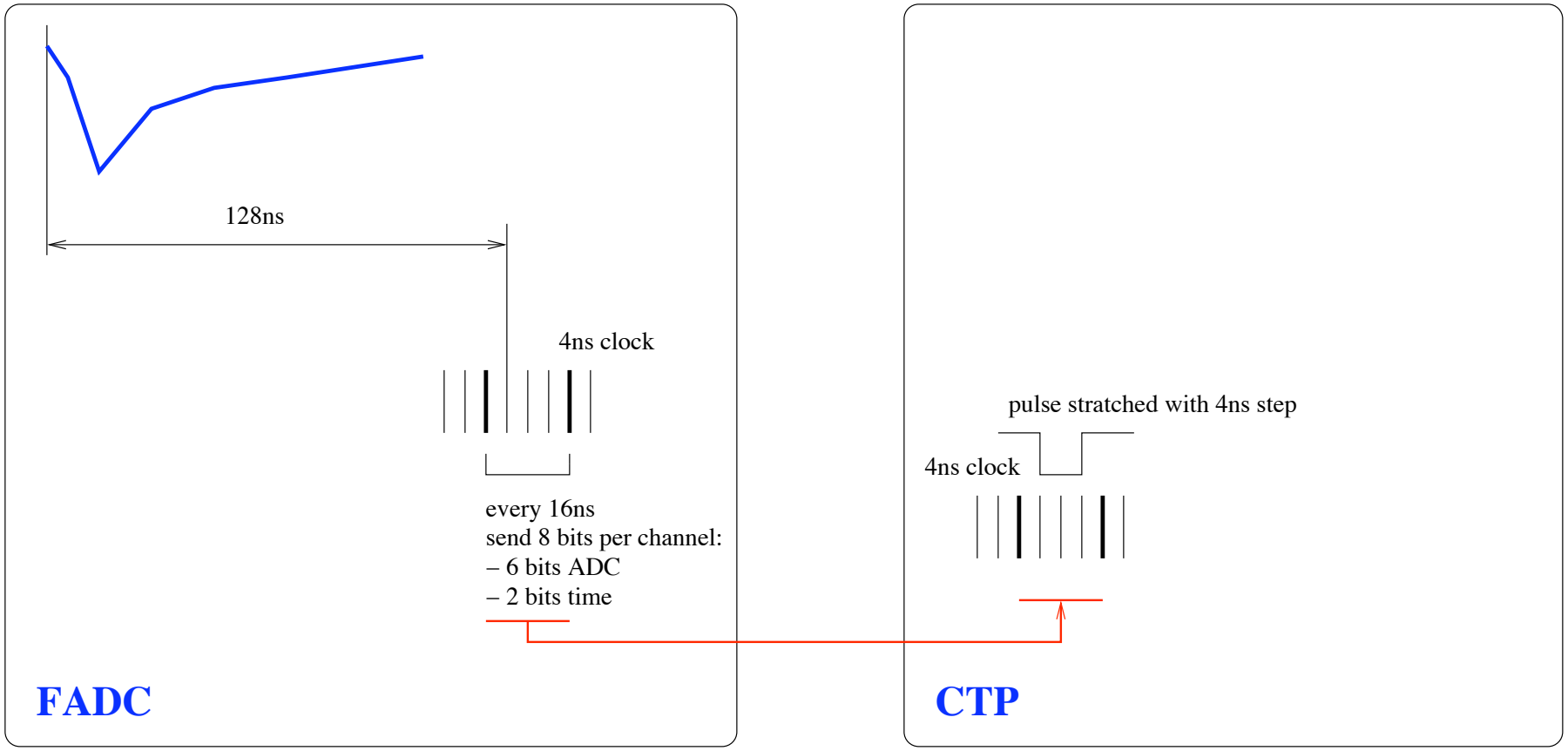
4. Based on bandwidth 8GBit/s we can send 8bits per channel every 16ns: 6bits for ADC value and 2 bits for timing inside 16ns interval to restore 4ns resolution

Flash ADC board signal processing logic

CTP board:

1. Does not have information about original sum window width
2. 4ns resolution after restoring original timing
3. Expands every window up to the value (programmable) big enough to enforce coincidence between different channels, 4ns min with 4ns step
4. Every channel has programmable delay (4ns step) and readable scaler

Trigger processing – FADC/CTP



Trigger processing - CTP/SSP

- Calorimeter: search for clusters using 3x3 crystals window
- Muon system: search for hits
- Trigger 1: two calorimeter clusters, cuts on geometry (with respect to beam) and energy (two thresholds)
- Trigger 2: two muon hits, cuts on geometry (upper and bottom) and energy (threshold)
- Possible problem: boundary effects because of segmented calorimeter readout and limited bandwidth between CTP and SSP

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Timeline

- Available boards: all TDCs, VME/VME64X crates
- Ordered by Nov 2010: 16 JLAB-made discriminator/scaler boards
- Ordered by Jan 2011: 16 FADCs, 3 CTPs, 3 SDs, 3 TIs, 3 Signal Distribution Boards
- Not ordered but needed: 32 FADC boards, 1 SSP board, VXS crates, crate controllers
- Oct 2010 - Jan 2011: FADC, CTP and SSP trigger FPGAs programing
- Feb 2011: testing starts with partially assembled system (without SVT readout)
- Feb 2011: SVT Board available
- April 2011: testing continues with SVT readout
- Jun 2011: complete DAQ/trigger system (without final SVT which is available in Fall

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